

Stony Brook University The Graduate School

Doctoral Defense Announcement

Abstract

Design and Implementation of Reconfigurable Hardware for Real Time Particle Filters

By

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Particle Filtering is a Monte Carlo sampling based signal processing technique that is applied to systems described using dynamic state space models. For models that are nonlinear and non-Gaussian, traditional filtering techniques fail in terms of filter performance. Particle filters can handle nonlinear and non-Gaussian systems much more efficiently than such methods. As a result, these filters have gained immense popularity in recent years. However, their high computational intensity, which is widely recognized in literature, makes them unsuitable for implementation on sequential platforms like DSPs. This fact, along with the absence of dedicated hardware for particle filtering has prevented their use in real time systems despite their suitability in terms of filter performance. The goal of this dissertation is to address this gap and develop hardware suitable to real time particle filtering. This research has led to the *first* FPGA prototype of a particle filter.

Often, real world systems require multiple models for accurate and complete description. A class of particle filters known as Multiple Model Particle Filters are applied to such systems. We provide extensions and modifications of the parallel architecture proposed for standard particle filters, for implementation of these multiple model particle filters.

Flexibility of particle filters is another of their widely recognized assets. Within a general framework, the particle filter can be applied to a wide range of problems in various fields by modification of certain filtering parameters. We exploit the concept of hardware reconfiguration to develop reconfigurable architectures, whereby the same particle filtering device can be used for different problems by simply specifying a set of parameters. Run time reconfiguration for implementation of multiple model particle filters with dynamically changing model sets is also explored.

For each of the hardware architecture proposed, an FPGA based evaluation of speed and resource requirement is performed and the overall improvements over a sequential DSP based implementation of the corresponding algorithm are analyzed.

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