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Abstract

Process development for high-speed superconductor microelectronics for digital and mixed signal applications

By

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After half a century of enormous successes and complete dominance, semiconductor electronics based on Si Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) is fast approaching its limits for high-end applications in telecommunications, computing and routing. Digital Superconductor electronics (SCE) based on the Rapid Single Flux Quantum Logic (RSFQ) has been considered as a viable low risk alternative to Si CMOS circuits, due to its potential in ultrahigh operating frequency and ultra-low power dissipation. The most developed and reliable superconductor electronics fabrication technology has been the one based on the externally shunted Nb/Al/AlO_x/Nb Josephson tunnel junctions (JJ). The technology level is characterized by the Nb/Al/AlO_x/Nb trilayer critical current density – jc, and the minimum junction size - a. The maximum clock frequency of the RSFQ-based SCE circuits scales as $(jc)^{1/2}$ or $1/a$. The main goals of the thesis work has been first to research the prevailing physical limitations of the existing methods of making SCE circuits and restrictions on the circuit complexity and speed; second to develop a reliable and scalable SCE fabrication process that is capable of making high-speed complex circuits for digital and mixed signal applications; and third to implement the results at a commercial SCE foundry at HYPRES Inc. To this end an advanced fabrication process with 4.5 kA/cm^2 JJ has been developed. The process is based on an enhanced lithography and thin film processes and incorporates addition anodization step for JJ protection. A simple approach for scaling of the existing circuit designs to newer higher jc processes has been proposed and implemented. A great number of complex digital circuits ($>10^4$ JJ) operating at clock frequencies in excess of 30 GHz has been fabricated for the first time as well as less complex (~ 500 JJs) circuits operating above 40 GHz and simple circuits (~ 20 JJs) operating at ~ 400 GHz. The maximum operating frequency as well as the complexity of SCE circuits has been doubled with respected to the previous state-of-the-art as a result of this work.

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